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SEP 03 2003
PATENT & TRADEMARK OFFICE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number: 09/885,792
Filing Date: 06/20/2001
Applicant: Basanth Jagannathan
5 Application Title: A NON-SELF-ALIGNED SiGe
HETEROJUNCTION BIPOLAR
TRANSISTOR
Examiner: Latin, Christopher W.
Art Unit: 2812

10 DECLARATION UNDER 37 CFR 1.131

Commissioner of Patents
P.O. BOX 1450
Alexandria, VA 22313-1450
Sir:

15

Basanth Jagannathan, Shwu-Jen Jeng, Jeffrey B. Johnson, Robb A. Johnson, Louis D. Lanzerotti, Kenneth J. Stein, and Seshadri Subbanna, applicants in the above-identified patent application, declare as follows:

- 20 1) During a period of time prior to September 1, 2000, the 35 USC 102(e) date of US patent 6,410,975 to Racanelli, we worked as a team and conceived of and reduced to practice the invention disclosed and claimed in the above-referenced application.
- 25 2) Specific proof of our conception and reduction to practice is evidenced by the attached Exhibit A (Disclosure FIS8-2000-0337), which is a confidential invention disclosure form used within the assignee corporation, IBM. The exhibit was prepared in preparation of a patent application. The work associated with the attached exhibit was the basis for the patent application referenced above.
- 30 3) Exhibit A describes and illustrates the non-self aligned transistor and fabrication method of the present invention. Specifically, Figs. 1a-1j of Exhibit A illustrate the prior art (also illustrated in Figs. 1A-1J in the present specification). Figs. 2a-2i of Exhibit A

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illustrate the method of the present invention, including steps of intrinsic base implant (Fig. 2g) and deposition of the nitride layer (Fig. 2d) that provides an implant mask over the emitter pedestal.

5 4) The discussion on page 6 of Exhibit A provides further evidence of conception and reduction to practice.

5) Exhibit A was last modified on June 27, 2000 (see the top of page 1). This Exhibit demonstrates both conception and reduction to practice of the invention prior to the filing
10 date of the Racanelli reference (September 1, 2000).

6) We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful, false statements so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity
15 of the above-referenced application and any patent issuing thereon.

Date 9/2/2003Basant Jagannathan Basant Jagannathan

20

Date Sept 2, 2003Shwu-Jen Jeng Shu-Jen Jeng

Date _____

Jeffrey B. Johnson _____

25 Date _____

Robb A. Johnson _____

Date _____

Louis D. Lanzerotti _____

30

Date 9-2-03Kenneth J. Stein Kenneth J.Date 9/2/03Seshadri Subbanna, Seshadri Subbanna

EXHIBIT A

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Disclosure FIS8-2000-0337

Created By: Shwu-Jen Jeng **Created On:** 09/07/99 02:14:47 PM
Last Modified By: Hilda Heinlein **Last Modified On:** 06/27/2000 05:19:53 PM

***** IBM Confidential *****

Required fields are marked with the asterisk (*) and must be filled in to complete the form.

Summary

Status	Under Evaluation
Processing Location	FIS
Functional Area	ZISA-Issac
Attorney/Patent Professional	Joseph Abate/Fishkill/IBM
IDT Team	Michael Hargrove/Fishkill/IBM; William Devine/Fishkill/IBM; Jack Mandelman/Fishkill/IBM; Louis Mysur/Fishkill/IBM; Peter Smeyers/Fishkill/IBM; DOMINIC SCHEPIS/Fishkill/IBM; Patricia A O'Neil/Fishkill/IBM
Submitted Date	08/27/2000 09:30:20 AM
Owning Division	MD
PVT Score	To calculate a PVT score, use the 'Calculate PVT' button.
Incentive Program	
Lab	
Technology Code	101NS

Inventors with Lotus Notes IDs

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FIS8-2000-0337 A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT) - continued

Response Due to PTC-07/27/2000

Main Idea

~~Ideas of disclosure or English~~

A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT)

~~Ideas of disclosure~~

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

Using a non-self aligned scheme to replace the emitter pedestal and self-aligned extrinsic base structure, the total process time and thermal cycle for the non-self aligned scheme will be reduced compared to the self-aligned structure. In the simplified process of forming the non-self aligned emitter, due to the reduced transient enhanced diffusion of the dopants much sharper and narrower doping profiles can be obtained. As a result, the transistor structure can be tailored for high-speed performance. The reduced process time also lowers the cost of fabricating the device.

A related advantage in this low thermal cycle processing is that it allows for making use of thin LTE layers to form base and collector regions. This leads to possibilities of even higher speed devices. The ability to integrate thin LTE layers in this structure also implies that the overall device topography can be lowered making MEOL processing much easier.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?

After LTE in-situ boron doped base been put down, a conventional dielectric emitter pedestal and a self-aligned extrinsic base spacer structure as shown in Figure 1j will require additional pedestal RIE, spacer deposition and etch, oxide strip, high pressure oxidation, and emitter opening RIE process steps before reaching emitter poly deposition.(The film thickness scaled down by approximately 20% from generation 5HP to generation 7HP.)

Insert text description of ETX process (5 and 6HP) for Figures 1a-1j.

- Sub-Collector
- Shallow Trench Isolation
- Reach-Through



Figure 1a.

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FIS8-2000-03S7 A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT) - continued



Figure 1b.

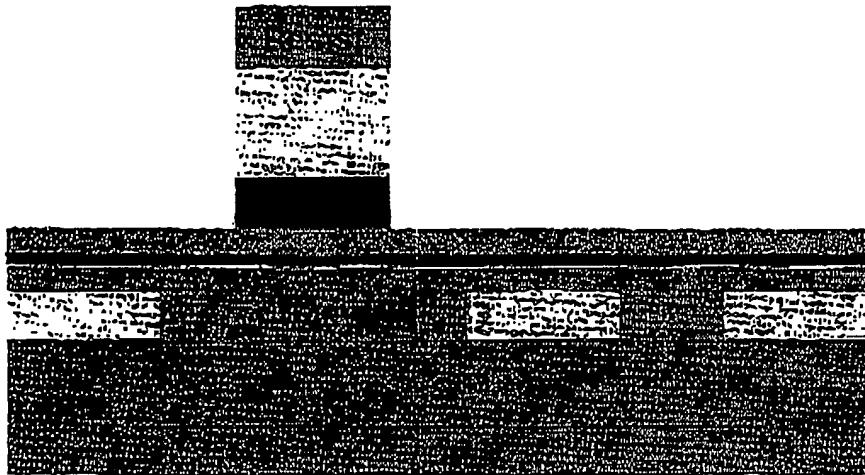


Figure 1c.

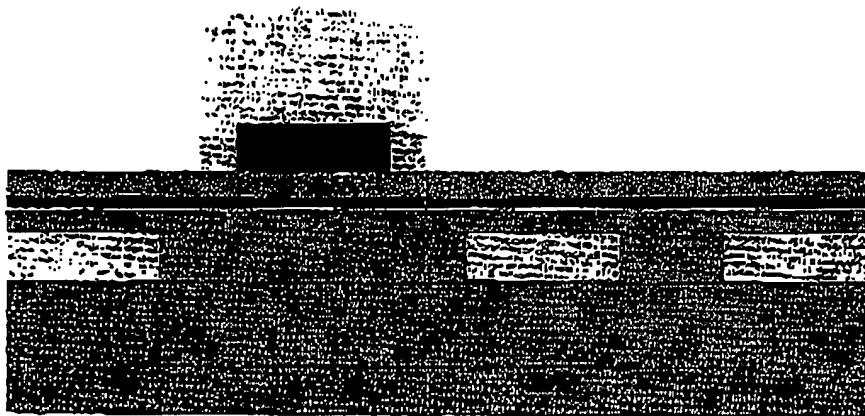


Figure 1d.

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FIS8-2000-0337 A Non-Self Aligned SiGe Heterofunction Bipolar Transistor (HBT) - continued

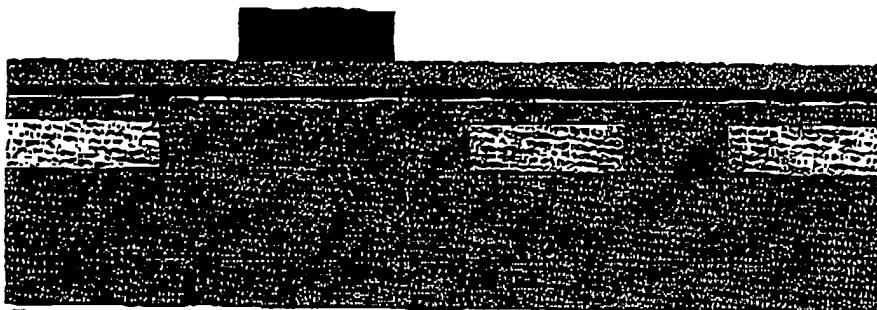


Figure 1e.

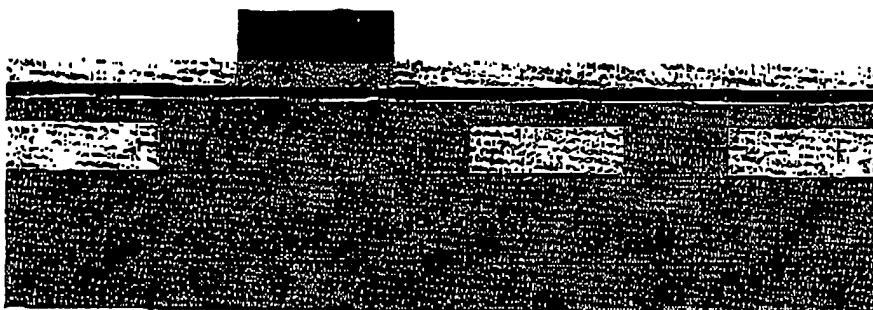


Figure 1f.



Figure 1g.

- Convert Polysilicon to Oxide
 - HiPOx

- Remove Nitride
- Remove Polysilicon
- Remove Nitride

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FIS8-2000-0337 A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT) - continued'

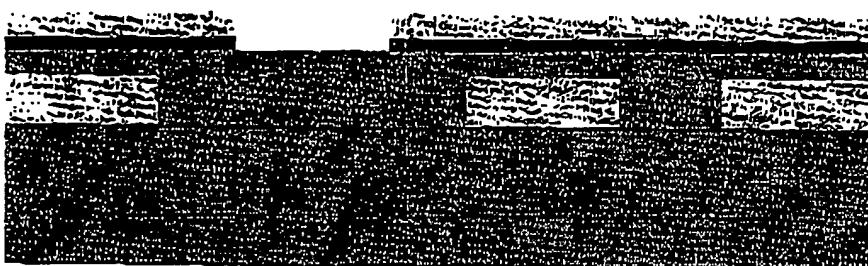


Figure 1h.

- Pedestal Implant for High f_t Device
 - Phosphorous
- Self-aligned to Extrinsic Base Implant

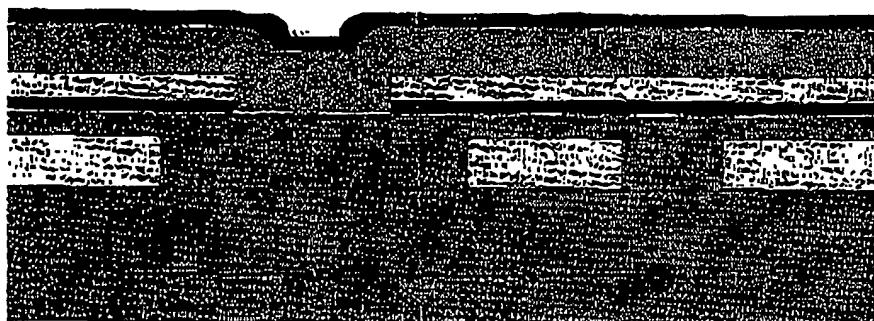


Figure 1i.

- Rapid Thermal Oxidation
- Emitter Polysilicon Deposition and Implant
 - Arsenic
- Protect Nitride
- Emitter RTA



Figure 1j.

- Emitter Photo and Etch
- Base Photo and Etch

As seen from the prior art the self-aligned process is complicated and time consuming. Using a non-self aligned structure, the complicated emitter pedestal is no longer needed. Instead, the emitter stack now consists of 100Å HIPOx, 500Å RTCVD nitride, and 700Å LPVCD or PECVD TEOS as shown in Figure 2a. (The 500Å RTCVD nitride can be replaced by an 800Å PECVD nitride to further reduce thermal cycle. This 800Å PECVD nitride will

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FISB-2000-0337 A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT) - continued

be reduced to 500Å after NP oxide strip to maintain some amount of parasitic capacitance.) Using a reverse polarity resist, the resist is developed at the emitter, and the emitter opening is defined by etching through 700Å TEOS as shown in Figure 2b. The resist is then stripped and the TEOS is then used as a hardmask to etch the 500Å nitride and stop at the 100Å HiPOx as shown in Figure 2c. Subsequently, the HiPOx is stripped (along with the hardmask), and an In-situ phosphorus doped emitter or an arsenic implanted emitter is formed as in Figure 2d. After the emitter poly is capped by nitride, the emitter is patterned and etched (Figure 2e). This is followed by patterning of the base region as in Figure 2f. Finally, the nitride-capped emitter poly is used as a mask for extrinsic base implant as shown in Figure 2g. In this case we use the PFET S/D implants for the extrinsic base doping rather than using a dedicated implant. This saves time and money. The advantage of non-self aligned structure is that no complicated emitter pedestal, spacer deposition and etch, HiPOx conversion process is required. However, the structure becomes more sensitive to alignment (relative to the self-aligned process) as shown in Figure 2h and Figure 2i. Extrinsic base resistance must be controlled by tightening the emitter poly to emitter opening photo tolerance.(LTE and emitter poly thickness will be scaled down from generation to generation.)



Figure 2a.

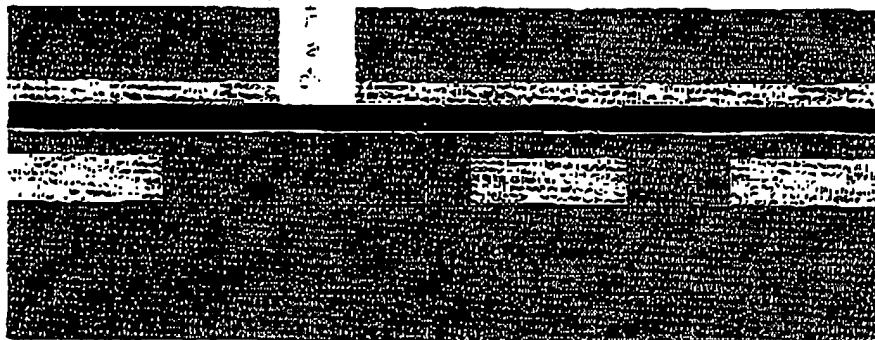


Figure 2b.

- EN Photo
 - Positive Photoresist
 - ARC
 - Standard EN Mask
- Etch Oxide (TEL)

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FIGS-2000-0397 A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT) - continued.

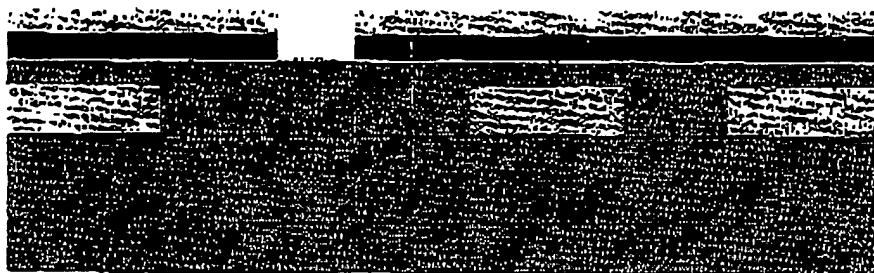


Figure 2c.

- Strip Resist
- Nitride Etch
 - Spacer chemistry
- Pedestal Implant

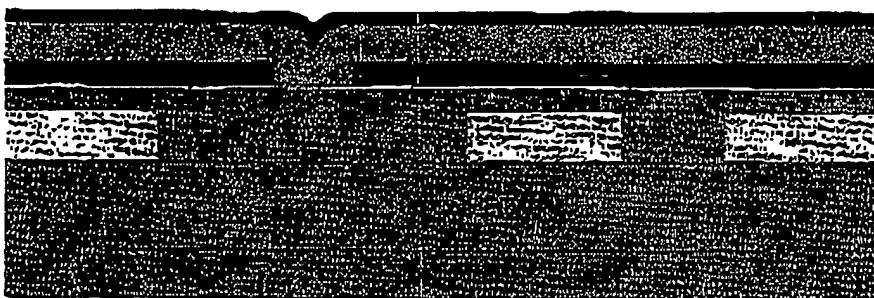


Figure 2d.

- RTO
- Emitter Polysilicon
- As⁺ Implant
- Nitride Protect

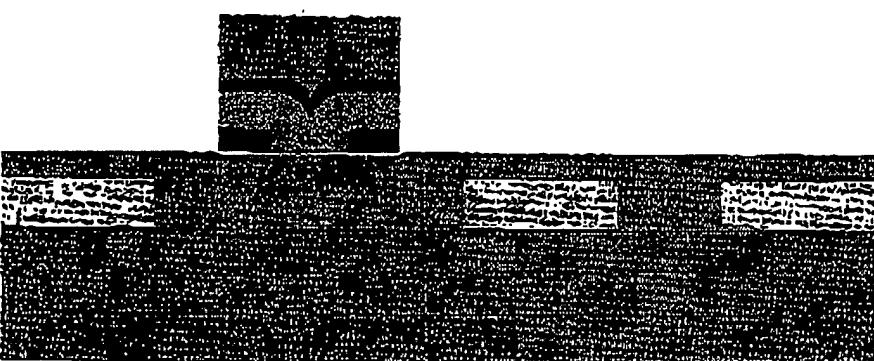


Figure 2e.

- NP Photo
- Etch Nitride
- Etch Polysilicon
- Etch Nitride

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FIS8-2000-0337 A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT) - continue



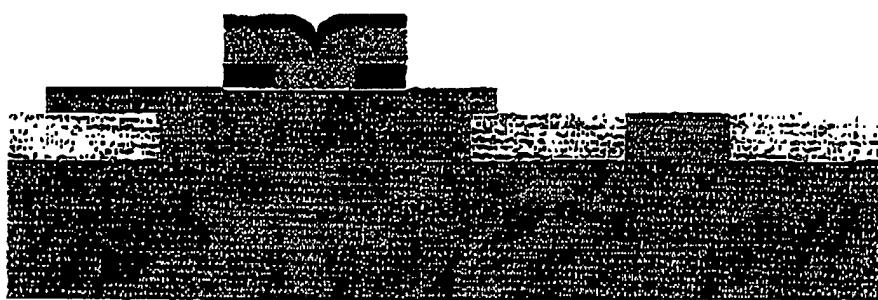
- **Base Etch Stopping on STI**

Figure 2f.



- **BN Photo**
- **Extrinsic Base Implant**
 - FET S/D (BN)

Figure 2g.



- **Perfectly aligned emitter polysilicon (NP) to emitter opening (EN) photo**

Figure 2h.

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FIS8-2003-0337 A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT) - continued

- Mis-aligned NP to EN photo

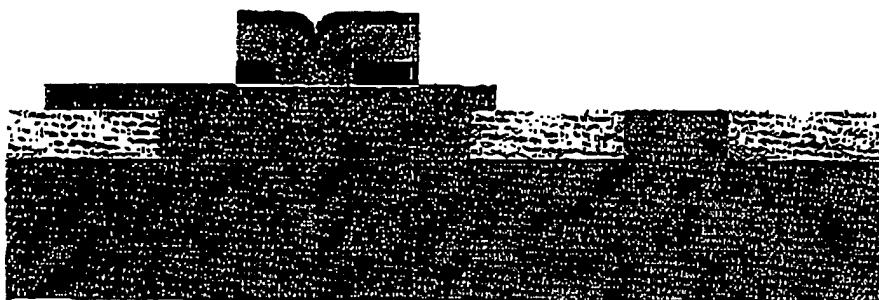


Figure 2i.

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.

***Critical Questions (Questions 1 - 7 must be answered)**

Question 1:

In what date was the invention workable? 06/05/2003 Please format the date as MM/DD/YY
Workable means i.e. when you know that your design will solve the problem.

Question 2:

Is there any planned or actual publication or disclosure of your invention to anyone outside IBM?

Yes

No

If yes, Enter the name of each publication or patent and the date published below:

Publication/Patent:

Date Published or Issued:

Are you aware of any publications, products or patents that relate to this invention?

Yes

No

If yes, Enter the name of each publication or patent and the date published below:

Publication/Patent:

Date Published or Issued:

Question 3:

Has the subject matter of the invention or a product incorporating the invention been sold, used internally in manufacturing, announced for sale, or included in a proposal?

Yes

No

Is a sale, use in manufacturing, product announcement, or proposal planned?

Yes

No

If Yes, Identify this product if known and indicate the date or planned date of sale, announcement, or proposal and to whom the sale, announcement or proposal has been or will be made.

Product:

Version/Release:

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F58-2000-0337 A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT) - continued

Code Name:

Date:

To whom:

If more than one, use cut and paste and append as necessary to the field provided.

Question 4:

Was the subject matter of your invention or a product incorporating your invention used in public? Yes No
 e.g., outside IBM or in the presence of non-IBMers?

If Yes, give a date. (Please format the date as MM/DD/YY/00)

Question 5:

Have you ever discussed your invention with others not employed at IBM?

If Yes, identify individuals and date discussed. Fill in this text area with the following information: the names of the individuals, the employer, date discussed, under CDA, and CPAC.

Question 6:

Was the invention in any way started or developed under a government contract or project?

If Yes, enter the contract number.

 Yes No Not Sure

Question 7:

Was the invention made in the course of any alliance, joint development or other contract activities?

 Yes No Not Sure

If Yes, enter the following: Name of Alliance, Contractor or Joint Developer

Contract ID number

Relationship contact name

Relationship contact E-mail

Relationship contact phone

Question 8:

Have you submitted, or are you aware of, any related disclosure submissions?

 Yes No

If Yes, please provide the title and stock or disclosure number below.

Question 9:

What type of companies do you expect to compete with inventions of this type? Check all that apply.

- Manufacturers of enterprise servers
- Manufacturers of entry servers
- Manufacturers of workstations
- Manufacturers of PC's
- Non-computer manufacturers
- Developers of operating systems
- Developers of networking software
- Developers of application software
- Integrated solution providers
- Service providers
- Other (Please specify below)
- mixed signal semiconductor companies

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Patent Value Tool (Optional - this may be used by the inventor and attorney to assist with the evaluation of your invention.)

(The Patent Value tool can be used by you or the evaluation team to determine the potential licensing value of your invention.)

The Patent Value Tool has not yet been used to calculate a score.

Post Disclosure Text & Drawings

Enter any additional information relating to this disclosure below:

(Form Revised 12/17/97)